EMI/EMC Compliant, ±15 kV ESD Protected, RS-232 Line Drivers/Receivers

ADM14196E

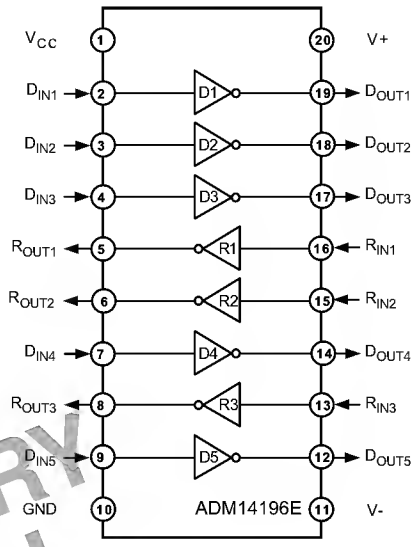
FEATURES

Complies with 89/336/EEC EMC Directive
ESD Protection to IEC1000-4-2 (801.2)
±8 kV: Contact Discharge
±15 kV: Air-Gap Discharge
±15 kV: Human Body Model
Fast Transient Burst (EFT) Immunity (IEC1000-4-4)
Low EMI Emissions (EN55022)
Eliminates Costly TransZorbs*
230 kbits/s Data Rate Guaranteed
Laplink®Compatible
Conforms to EIA/TIA-232-E
5 Drivers and 3 Receivers
Complements ADM14185E (3 Drivers/5 Receivers)
Flow-through Pinout
Failsafe Receiver Outputs
Rugged Replacement for DS14196

APPLICATIONS

Personal Computers
Printers
Peripherals
Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM14196E is a robust RS-232 and V.28 interface device which operates from +5V and ±12V power supplies. It is suitable for operation in harsh electrical environments and is compliant with the EU directive on EMC (89/336/EEC). Both the level of emissions and immunity are in compliance. EM immunity includes ESD protection in excess of ±15 kV on all I-O lines (1000-4-2), Fast Transient Burst protection (1000-4-4) and Radiated Immunity (1000-4-3). EM emissions include radiated and conducted emissions as required by Information Technology Equipment EN55022, CISPR22.

All devices fully conform to the EIA-232E and CCITT V.28 specifications and operate at data rates up to 230 kbps.

The ADM14196E is available in 20-pin SO package.

*TransZorb is a registered trademark of General Semiconductor Industries, Inc.

REV. 0

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ADM14196E–SPECIFICATIONS

(V_{CC} = 4.75V to 5.25V, V+ = 9.0V to 13.2V, V- = -9.0V to -13.2V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} Power Supply Current		250	500	µA	No Load, All Inputs at +5V
V+ Power Supply Current (Note 1)		175	300	µA	No Load, All Driver Inputs at 0.8V or 2V, All Receiver Inputs at 0.8V or 2.4V
V- Power Supply Current (Note 1)		-150	-300	µA	
Driver CMOS Inputs					
High Level Input Voltage, V_{INH}	2.0			V	
Low Level Input Voltage, V_{INL}			0.8	V	
High Level Input Current I_{INH} (Note 1)			1	µA	V_{IN} = 5V
Low Level Input Current I_{INL} (Note 1)			-1	µA	V_{IN} = 0V
Driver EIA-232 Outputs					
High Level Output Voltage, V_{OH} (Note 1)	6	7		V	RL = 3kΩ, V_{IN} = 0.8V, V+ = 9V, V- = -9V
	8.5	10		V	RL = 3kΩ, V_{IN} = 0.8V, V+ = 12V, V- = -12V
	10	11.5		V	RL = 7kΩ, V_{IN} = 0.8V, V+ = 13.2V, V- = -13.2V
Low Level Output Voltage, V_{OL} (Note 1)		-7	-6	V	RL = 3kΩ, V_{IN} = 2V, V+ = 9V, V- = -9V
		-8	-7.5	V	RL = 3kΩ, V_{IN} = 2V, V+ = 12V, V- = -12V
		-11	-10	V	RL = 3kΩ, V_{IN} = 2V, V+ = 13.2V,V- = -13.2V
Output High Short-Circuit Current I_{OS+}	-6	-13	-18	mA	V_O = 0V, V_{IN} = 0.8V(Note 1)
Output Low Short-Circuit Current I_{OS-}	6	13	18	mA	V_O = 0V, V_{IN} = 2.0V(Note 1)
Output Resistance	300			Ω	-2V ≤ V_O ≤ +2V, V+ = V- = V_{CC} = 0V
Output Resistance	300			Ω	-2V ≤ V_O ≤ +2V, V+ = V- = V_{CC} = Open Cct
Receiver EIA-232 Inputs					
Input High Threshold, V_{TH} (Recognized as a High Signal)		2.0	2.4	V	V_O ≤ 0.4V, I_O = 3.2mA
Input Low Threshold, VTL (Recognised as a Low Signal)	0.8	1.0		V	V_O ≥ 2.5V, I_O = -0.5mA
Input Resistance R_{IN}	3.0	5.0	7.0	kΩ	V_{IN} = ±3V to ±15V
Input Current I_{IN} (Note 1)	2.1	3.0	5.0	mA	V_{IN} = +15V
	0.43	0.6	1	mA	V_{IN} = +3V
	-5.0	-3.0	-2.1	mA	V_{IN} = -15V
	-1	-0.6	-0.43	mA	V_{IN} = -3V
Receiver CMOS Outputs					
High Level Output Voltage, V_{OH} (Note 1)	4.0	4.5		V	I_{OH} = -1.0mA, V_{CC}=5V, V_{IN} = -3V
	4.5	4.9		V	I_{OH} = -10µA,V_{CC}=5V, V_{IN} = -3V
	4.0	4.5		V	I_{OH} = -1.0mA, V_{CC}=5V, V_{IN} = Open Circuit
	4.5	4.9		V	I_{OH} = -10µA, V_{IN} = Open Circuit
Low Level Output Voltage, V_{OL}		0.2	0.4	V	I_{OL} = 3.2mA, V_{IN} = +3V
Short-Circuit Current I_{OSR} (Note 1)		±10		mA	V_O = 0V, V_{IN} = 0V
Driver Switching Characteristics					
Propagation Delay High to Low, T_{PHL}		1.2	1.5	µs	
Propagation Delay, Low to High, T_{PLH}		1.2	1.5	µs	R_L = 3kΩ, C_L = 50pF (*Figures 2 and 3*)
Output Rise and Fall Time, t_r, t_f (Note 7)		0.3		µs	
Receiver Switching Characteristics					
Propagation Delay High to Low, T_{PHL}		250	500	ns	R_L = 3kΩ, C_L = 15pF (Includes fixture plus probe)
Propagation Delay, Low to High, T_{PLH}		400	800	ns	
Output Rise Time, t_r		15	50	ns	(*Figures 4 and 5*)
Output Fall Time, t_f		15	50	ns	

ADM14196E–SPECIFICATIONS

(V_{CC} = 4.75V to 5.25V, V+ = 9.0V to 13.2V, V- = -9.0V to -13.2V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
ESD and EMC					
ESD Protection (I-O Pins)		±15		kV	Human Body Model
		±15		kV	IEC1000-4-2 Air Discharge
		±8		kV	IEC1000-4-2 Contact Discharge
ESD Protection (All Other Pins)		±2.5		kV	Human Body Model, MIL-STD-883B
EFT Protection (I-O Pins)		±2		kV	IEC1000-4-4
EMI Immunity		10		V/m	IEC1000-4-3

Specifications subject to change without notice.

Notes

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referred to ground unless otherwise specified. For current, minimum and maximum values are specified as an absolute value and the sign is used to indicate direction. For voltage logic levels, the more positive value is designated as maximum. For example, if -6V is a maximum, the typical value (-6.8V) is more negative.
2. All typicals are given for V_{CC} = +5.0V, V+ = +12.0V, V- = -12.0V, T_A = 25°C.
3. Only one driver output shorted at a time.
4. Generator characteristics for driver input: f = 64kHz (128 kbits/sec), $t_r = t_f$ = 10ns, V_{INH} = 3V, V_{INL} = 0V, duty-cycle = 50%.
5. Generator characteristics for receiver input: f = 64kHz (128 kbits/sec), $t_r = t_f$ = 200ns, V_{INH} = 3V, V_{INL} = -3V, duty-cycle = 50%.
6. If receiver inputs are unconnected, receiver output is a logic high.
7. Refer to typical curves. Driver output slew rate is measured from the +3.0V to the -3.0V level on the output waveform. Inputs not under test are connected to VCC or GND. Slew rate is determined by load capacitance. To comply with a 30V/µs maximum slew rate, a minimum load capacitance of 390pF is recommended.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} ..... –0.3 V to +7 V
V+ ..... (V_{CC} –0.3 V) to +15 V
V– ..... +0.3 V to –15 V
Input Voltages
  Driver Inputs D_{IN} ..... –0.3 V to (V+, +0.3 V)
  Receiver Inputs R_{IN} ..... ±25 V
Output Voltages
  Driver Outputs D_{OUT} ..... ±15 V
  Receiver Outputs R_{OUT} .. –0.3 V to (V_{CC} +0.3 V)
Short Circuit Duration
  D_{OUT} ..... Continuous
Power Dissipation
  R-20 SOIC (Derate 12 mW/°C Above +70°C) 1488 mW
Operating Temperature Range
  Industrial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
ESD Rating (MIL-STD-883B) (I-O Pins) .....±15 kV
ESD Rating (MIL-STD-883B) (Except I-O) .. ±2.5 kV
ESD Rating (IEC1000-4-2 Air) (I-O Pins) .....±15 kV
ESD Rating (IEC1000-4-2 Contact) (I-O Pins) ..±8 kV
EFT Rating (IEC1000-4-4) (I-O Pins) .....±2 kV

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PIN FUNCTION DESCRIPTION

Pin Number	Mnemonic	Function
1	V_{CC}	Positive Logic Power Supply (4.75 to 5.25V)
2	R_{IN1}	Receiver Input (EIA-232 Signal levels)
3	R_{IN2}	Receiver Input (EIA-232 Signal levels)
4	R_{IN3}	Receiver Input (EIA-232 Signal levels)
5	D_{OUT1}	Driver Output (EIA-232 Signal levels)
6	D_{OUT2}	Driver Output (EIA-232 Signal levels)
7	R_{IN4}	Receiver Input (EIA-232 Signal levels)
8	D_{OUT3}	Driver Output (EIA-232 Signal levels)
9	R_{IN5}	Receiver Input (EIA-232 Signal levels)
10	V-	Negative Power Supply (-9 to -13.2V)
11	GND	Ground Pin. Must be connected to 0V
12	R_{OUT5}	Receiver Output (5V TTL/CMOS logic levels)
13	D_{IN3}	Driver Input (5V TTL/CMOS logic levels)
14	R_{OUT5}	Receiver Output (5V TTL/CMOS logic levels)
15	D_{IN3}	Driver Input (5V TTL/CMOS logic levels)
16	D_{IN3}	Driver Input (5V TTL/CMOS logic levels)
17	R_{OUT5}	Receiver Output (5V TTL/CMOS logic levels)
18	R_{OUT5}	Receiver Output (5V TTL/CMOS logic levels)
19	R_{OUT5}	Receiver Output (5V TTL/CMOS logic levels)
20	V+	Positive Power Supply (9V to 13.2V) .

ORDERING GUIDE

Model	Temperature Range	Package Option
ADM14196EAR	–40°C to +85°C	R-20

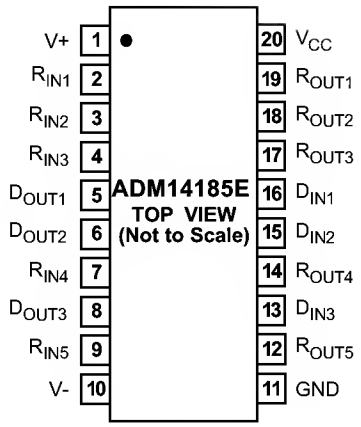


Figure 1. ADM14196E Pin Configuration

AC Characteristics

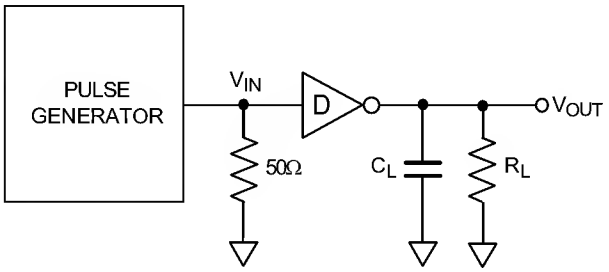


Figure 2. Test Circuit for Driver Propagation Delay and Transition Time

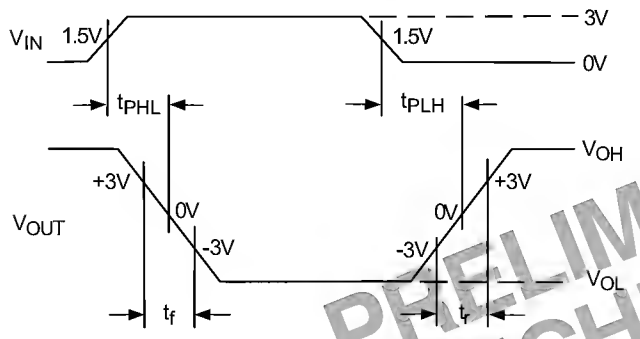


Figure 3. Driver Propagation Delay and Transition Time Waveforms

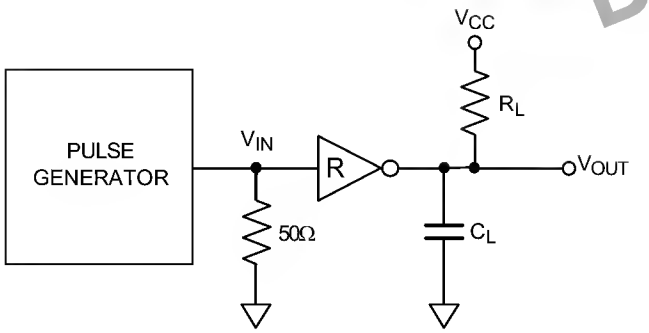


Figure 4. Test Circuit for Receiver Propagation Delay and Transition Time

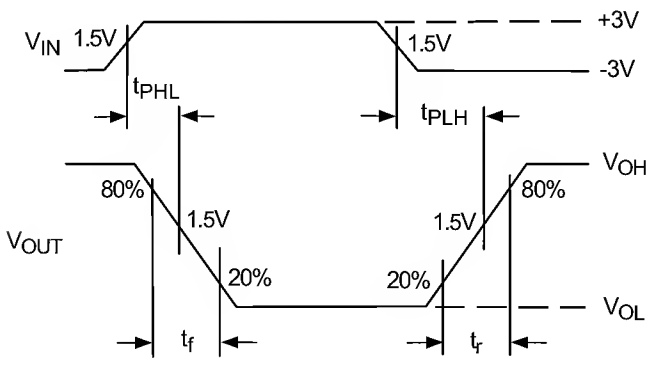


Figure 5. Receiver Propagation Delay and Transition Time Waveforms

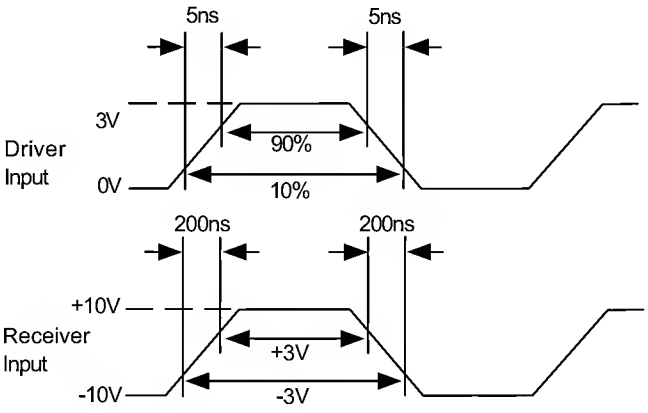


Figure 6. Input Waveforms Used in AC Performance Tests

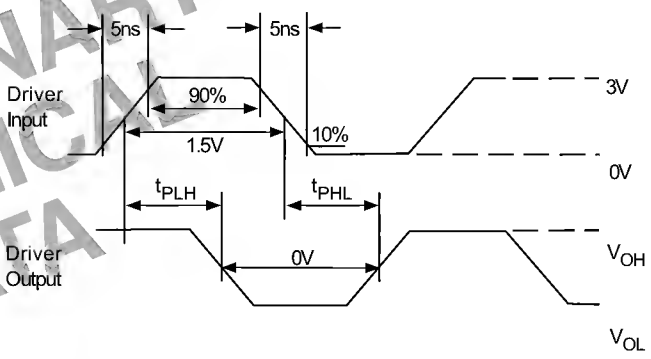


Figure 7. Input/Output Waveforms for Driver Propagation Delays vs. C_L

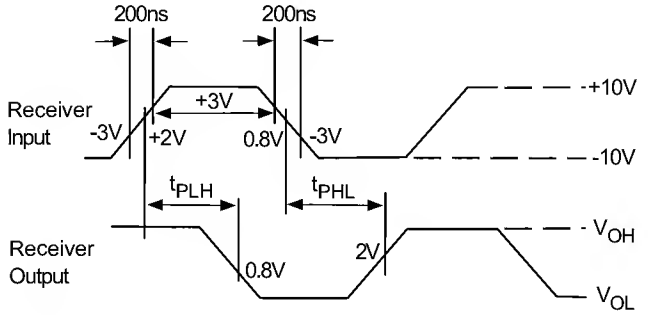


Figure 8. Input/Output Waveforms for Receiver Propagation Delay vs. C_L

Typical Performance Curves

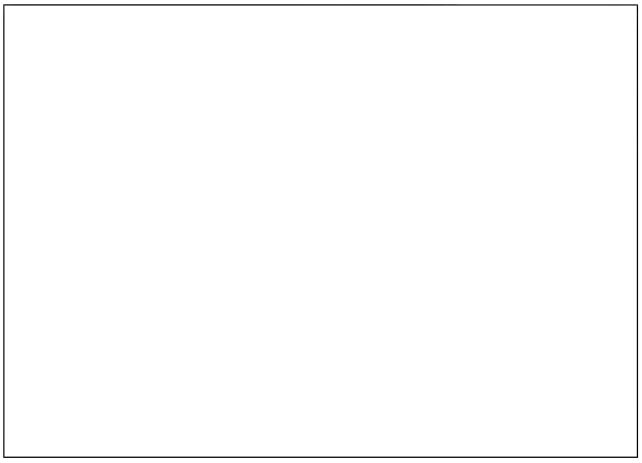


Figure 9. Driver Propagation Delay vs. C_L

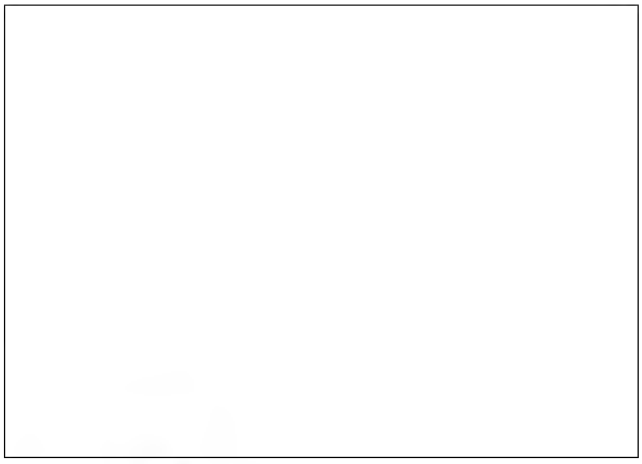


Figure 12. Driver Output Voltage vs. Frequency for C_L = 380pF and 2500pF

Figure 10. Receiver Propagation Delay vs. C_L

Figure 13. Supply Current vs. Frequency, One Receiver Switching

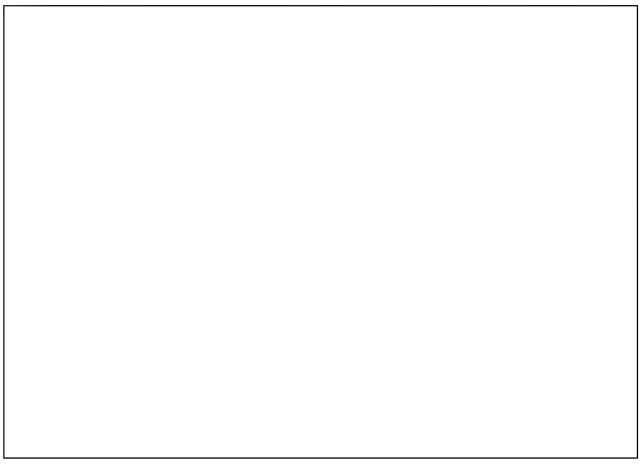


Figure 11. Driver Output Slew rate Between +3V and -3V vs C_L

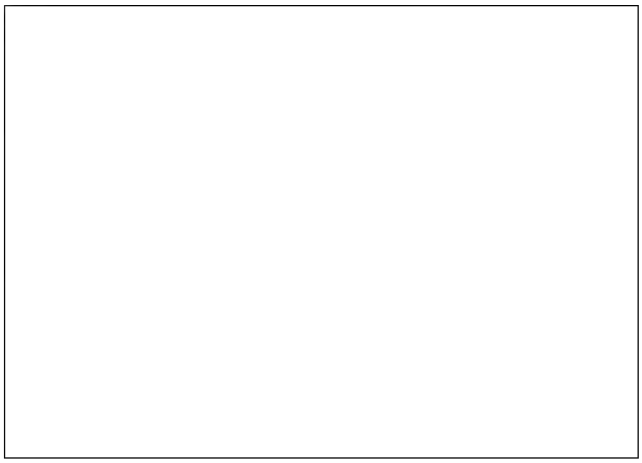


Figure 14. Supply Current vs. Frequency and CL, One Driver Switching

Typical Performance Curves

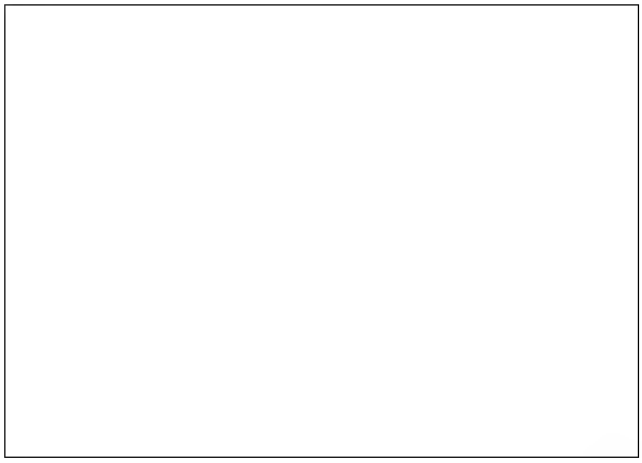


Figure 15. Supply Current vs Frequency and C_L, All Drivers and Receivers Switching

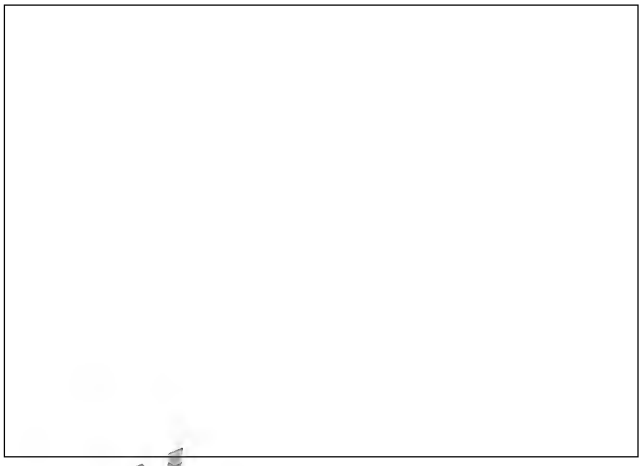


Figure 18. EMC Radiated Emissions

Figure 16. Driver Output Voltage vs. Output Current

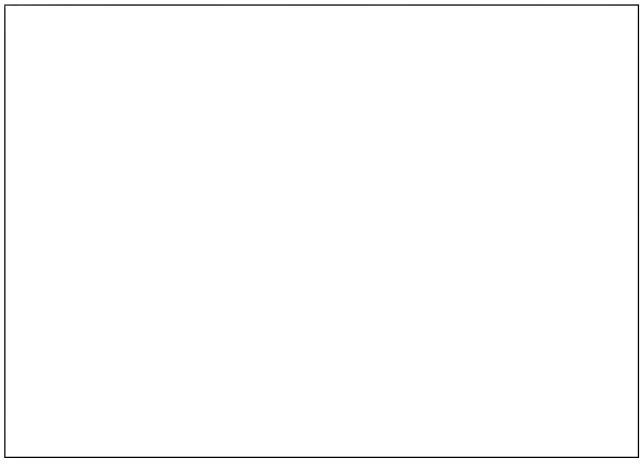


Figure 17. EMC Conducted Emissions

GENERAL DESCRIPTION

The AD14185E is a ruggedized RS-232 line driver/ receiver which operates from +5 V and ±12V supplies. It contains 5 receivers and 3 drivers, and provides a one-chip solution for 9-pin serial interfaces between data terminal and data communications equipment.
Features include low power consumption, high transmission rates and compatibility with the EU directive on electromagnetic compatibility. EM compatibility includes protection against radiated and conducted interference including high levels of electrostatic discharge.

All RS-232 inputs and outputs contain protection against electrostatic discharges up to ±15 kV and electrical fast transients up to ±2 kV. This ensures compliance to IE1000-4-2 and IEC1000-4-4 requirements.

This device is ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently being plugged/unplugged. They are also immune to high RF field strengths without special shielding precautions. Emissions are also controlled to within very strict limits.

CIRCUIT DESCRIPTION

The internal circuitry consists of three main sections. These are:

1. 5 V logic to EIA-232 transmitters.
2. EIA-232 to 5 V logic receivers.
3. Transient protection circuit on all I-O lines.

Transmitter (Driver) Section

The drivers convert 5 V logic input levels into EIA-232 output levels. With V_{CC} = +5 V, V+ = 12V, V- = -12V, and driving an EIA-232 load, the output voltage swing is typically ±10 V.

Unused inputs may be left unconnected, as an internal 400 ký pull-up resistor pulls them high forcing the outputs into a low state. The input pull-up resistors typically source 8 µA when grounded, so unused inputs should either be connected to V_{CC} or left unconnected in order to minimize power consumption.

Receiver Section

The receivers are inverting level shifters which accept EIA-232 input levels and translate them into 5 V logic output levels.
The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±25 V. The guaranteed switching thresholds are 0.4 V minimum and 2.4 V maximum. Unconnected inputs are pulled to 0 V by the internal 5 kΩ pull-down resistor. This, therefore, results in a Logic 1 output level for unconnected inputs or for inputs connected to GND.

The receivers have Schmitt trigger input with a hysteresis level of 0.5 V. This ensures error-free reception for both noisy inputs and for inputs with slow transition times.

High Baud Rate

The AD14185E features high slew rates permitting data transmission at rates well in excess of the EIA-232-E specifications. RS-232 levels are maintained at data rates up to 230 kb/s even under worst case loading conditions. This allows for high speed data links between two terminals or indeed it is suitable for the new generation modem standards which requires data rates of 200 kb/s. The slew rate is internally controlled to less than 30 V/µs in order to minimize EMI interference.

ESD/EFT Transient Protection Scheme.

The AD14185E uses protective clamping structures on all inputs and outputs which clamps the voltage to a safe level and dissipates the energy present in ESD (Electrostatic) and EFT (Electrical Fast Transients) discharges. A simplified schematic of the protection structure is shown in Figures 19 and 20. Each input and output contains two back-to-back high speed clamping diodes. During normal operation with maximum RS-232 signal levels, the diodes have no affect as one or the other is reverse
biased depending on the polarity of the signal. If however the voltage exceeds about ±50 V, reverse breakdown occurs and the voltage is clamped at this level. The diodes are large p-n junctions which are designed to handle the instantaneous current surge which can exceed several amperes.

The transmitter outputs and receiver inputs have a similar protection structure. The receiver inputs can also dissipate some of the energy through the internal 5 kΩ resistor to GND as well as through the protection diodes.

The protection structure achieves ESD protection up to ±15 kV and EFT protection up to ±2 kV on all RS-232 I-O lines. The methods used to test the protection scheme are discussed later.

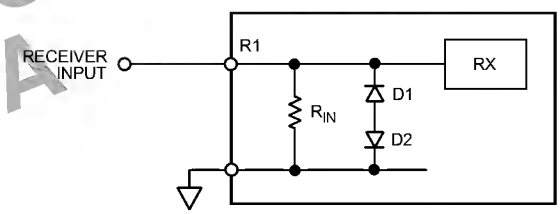


Figure 19. Receiver Input Protection Scheme

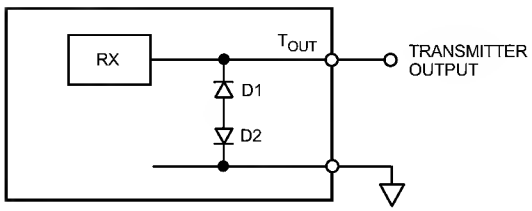


Figure 20. Transmitter Output Protection Scheme

ESD TESTING (IEC1000-4-2)

IEC1000-4-2 (previously 801-2) specifies compliance testing using two coupling methods, contact discharge and air-gap discharge. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved towards the unit under test developing an arc across the air gap, hence the term air-discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method while less realistic is more repeatable and is gaining acceptance in preference to the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time coupled with high voltages can cause failures in unprotected semiconductors. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

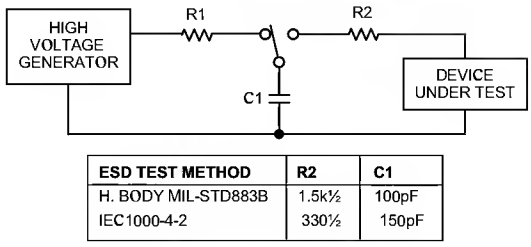
I-O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I-O cable can result in a static discharge which can damage or completely destroy the interface product connected to the I-O port. Traditional ESD test methods such as the MIL-STD-883B method 3015.7 do not fully test a products susceptibility to this type of discharge. This test was intended to test a products susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the traditional test and the IEC test:

(a) The IEC test is much more stringent in terms of discharge energy. The peak current injected is over four times greater.

(b) The current rise time is significantly faster in the IEC test.

(c) The IEC test is carried out while power is applied to the device.

It is possible that the ESD discharge could induce latch-up in the device under test. This test therefore is more representative of a real-world I-O discharge where the equipment is operating normally with power applied. For maximum peace of mind however, both tests should be performed, therefore, ensuring maximum protection both during handling and later during field service.



ESD TEST METHOD	R2	C1
H. BODY MIL-STD883B	1.5k½	100pF
IEC1000-4-2	330½	150pF

Figure 21. ESD Test Standards

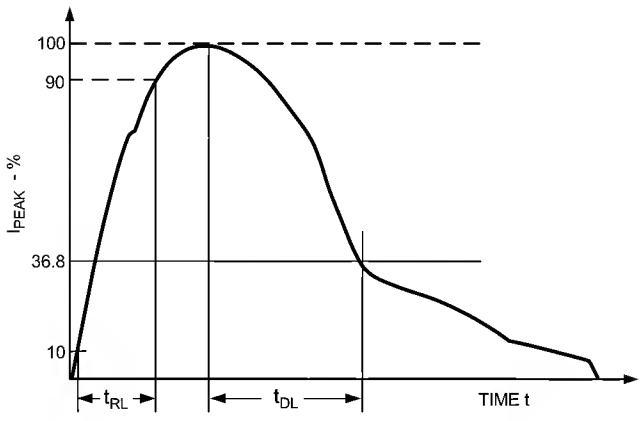


Figure 22. Human Body Model ESD Current Waveform

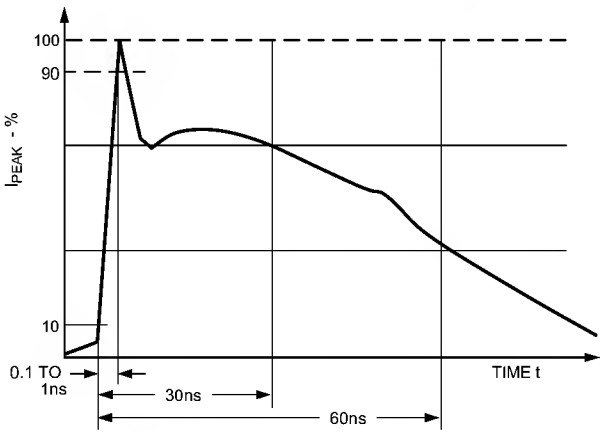


Figure 23. IEC1000-4-2 ESD Current Waveform

The ADM14196E is tested using both the above mentioned test methods. All pins are tested with respect to all other pins as per the MIL-STD-883B specification. In addition all I-O pins are tested as per the IEC test specification. The products were tested under the following conditions:

(a) Power-On—Normal Operation

(b) Power-Off

There are four levels of compliance defined by IEC1000-4-2. The ADM14196E meets the most stringent compliance level for both contact and for air-gap discharge. This means that the products are able to withstand contact discharges in excess of 8 kV and air-gap discharges in excess of 15 kV.

Table IV. IEC1000-4-2 Compliance Levels

Level	Contact Discharge kV	Air Discharge kV
1	2	2
2	4	4
3	6	8
4	8	15

Table V. ADM14196E ESD Test Results

ESD Test Method	I-O Pins	Other Pins
MIL-STD-883B	±15 kV	±2.5 kV
IEC1000-4-2		
Contact	±8 kV	
Air	±15 kV	

FAST TRANSIENT BURST TESTING (IEC1000-4-4)

IEC1000-4-4 (previously 801-4) covers electrical fast-transient/burst (EFT) immunity. Electrical fast transients occur as a result of arcing contacts in switches and relays. The tests simulate the interference generated when for example a power relay disconnects an inductive load. A spark is generated due to the well known back EMF effect. In fact the spark consists of a burst of sparks as the relay contacts separate. The voltage appearing on the line, therefore, consists of a bust of extremely fast transient impulses. A similar effect occurs when switching on fluorescent lights.

The fast transient burst test defined in IEC1000-4-4 simulates

this arcing and its waveform is illustrated in Figure 24. It consists of a burst of 2.5 kHz to 5 kHz transients repeating at 300 ms intervals. It is specified for both power and data lines.

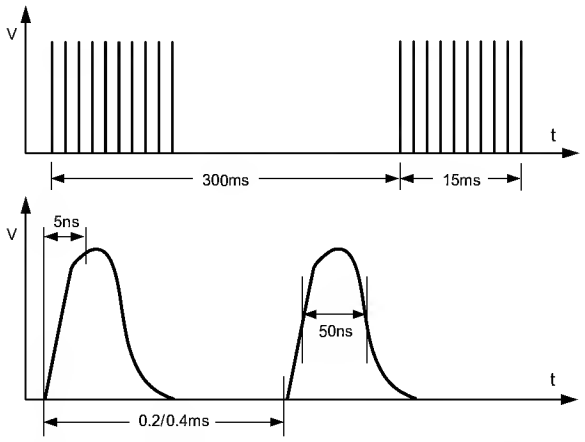


Figure 24. IEC1000-4-4 Fast Transient Waveform

Table VI.

(kV) Level	V Peak (kV) PSU	V Peak I-O
1	0.5	0.25
2	1	0.5
3	2	1
4	4	2

A simplified circuit diagram of the actual EFT generator is illustrated in Figure 25.

The transients are coupled onto the signal lines using an EFT coupling clamp. The clamp is 1 m long and it completely surrounds the cable providing maximum coupling capacitance
(50 pF to 200 pF typ) between the clamp and the cable. High energy transients are capacitively coupled onto the signal lines. Fast rise times (5 ns) as specified by the standard result in very effective coupling. This test is very severe since high voltages are coupled onto the signal lines. The repetitive transients can often cause problems where single pulses don't. Destructive latch-up may be induced due to the high energy content of the transients. Note that this stress is applied while the interface products are powered up and are transmitting data. The EFT test applies hundreds of pulses with higher energy than ESD. Worst case transient current on an I-O line can be as high as 40A.

Test results are classified according to the following:

1. Normal performance within specification limits.
2. Temporary degradation or loss of performance which is self-recoverable.
3. Temporary degradation or loss of function or performance which requires operator intervention or system reset.
4. Degradation or loss of function which is not recoverable due to damage.

The ADM14196E has been tested under worst case conditions using unshielded cables and meet Classification 2. Data transmission during the transient condition is corrupted but it may be resumed immediately following the EFT event without user intervention.

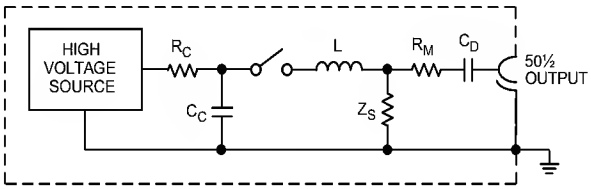


Figure 25. IEC1000-4-4 Fast Transient Generator

IEC1000-4-3 RADIATED IMMUNITY

IEC1000-4-3 (previously IEC801-3) describes the measurement method and defines the levels of immunity to radiated electromagnetic fields. It was originally intended to simulate the electromagnetic fields generated by portable radio transceivers or any other device which generates continuous wave radiated electromagnetic energy. Its scope has since been broadened to include spurious EM energy which can be radiated from fluorescent lights, thyristor drives, inductive loads, etc.

Testing for immunity involves irradiating the device with an EM field. There are various methods of achieving this including use of anechoic chamber, stripline cell, TEM cell, GTEM cell. A stripline cell consists of two parallel plates with an electric field developed between them. The device under test is placed within the cell and exposed to the electric field. There are three severity levels having field strengths ranging from 1 V to 10 V/m. Results are classified in a similar fashion to those for IEC1000-4-4.

1. Normal operation.
2. Temporary degradation or loss of function which is self-recoverable when the interfering signal is removed.
3. Temporary degradation or loss of function which requires operator intervention or system reset when the interfering signal is removed.
4. Degradation or loss of function which is not recoverable due to damage.

The ADM14196E easily meets Classification 1 at the most stringent (Level 3) requirement. In fact field strengths up to 30 V/m showed no performance degradation and error-free data transmission continued even during irradiation.

Table VII. Test Severity Levels (IEC1000-4-3)

Level	Field Strength V/m
1	1
2	3
3	10

EMISSIONS/INTERFERENCE

EN55 022, CISPR22 defines the permitted limits of radiated and conducted interference from Information Technology (IT) equipment. The objective of the standard is to minimize the level of emissions both conducted and radiated.

For ease of measurement and analysis, conducted emissions are assumed to predominate below 30 MHz and radiated emissions are assumed to predominate above 30 MHz.

CONDUCTED EMISSIONS

This is a measure of noise which gets conducted onto the line power supply. Conducted noise can be generated when device outputs switch, particularly if the P-channel output transistor switches on before the N-channel device switches off, or vice versa, drawing large current pulses from the power supply. Care is taken in the design of the ADM1485E to ensure that this does not happen. Conducted emissions are measured by monitoring the line power supply. The equipment used consists of a LISN (Line Impedance Stabilizing Network) which essentially presents a fixed impedance at RF, and a spectrum analyzer. The spectrum analyzer scans for emissions up to 30 MHz and a plot for the ADM14196E is shown in Figure 26.

Figure 26. Conducted Emissions Plot

RADIATED EMISSIONS

Radiated emissions are measured at frequencies in excess of 30 MHz. RS-232 outputs designed for operation at high baud rates while driving cables can radiate high frequency EM energy. The reasons already discussed which cause conducted emissions can also be responsible for radiated emissions. Fast RS-232 output transitions can radiate interference, especially when lightly loaded and driving unshielded cables.

The RS-232 outputs on the ADM14196E products feature a controlled slew rate in order to minimize the level of radiated emissions, yet are fast enough to support data rates up to 230 kBaud.

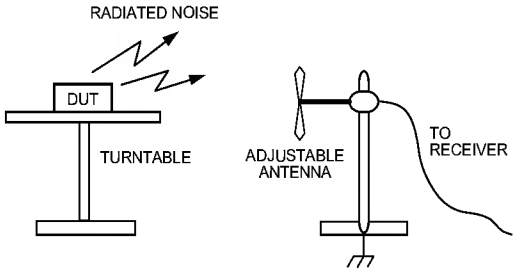


Figure 27. Radiated Emissions Test Setup

Figure 28 shows a plot of radiated emissions vs. frequency. This shows that the levels of emissions are well within specifications without the need for any additional shielding or filtering components. The ADM14196E was operated at maximum baud rates and configured as in a typical RS-232 interface.

Testing for radiated emissions was carried out in a shielded anechoic chamber.

Figure 28. Radiated Emissions Plot

APPLICATIONS INFORMATION

In a typical Data Terminal Equipment (DTE) to Data Circuit Terminating Equipment (DCE) 9-pin de facto interface implementation, 2 data lines (TXD and RXD) and 6 control lines (RTS, DTR, DSR, CTS and RI) are required. With its 5 drivers and 3 receivers, the ADM14196E offers a single chip solution for the DCE side of the interface.

As shown in figure 29, the flow-through pinout of the device allows for a very simple PCB layout. This simple layout allows a ground plane to be placed beneath the IC, and ground lines to be inserted between the signal lines to minimise crosstalk, without the complication of multi-layer PCBs.

For the DTE side of the interface, the complementary device (ADM14185E) with its 3 drivers and 5 receivers, may be used.

FAILSAFE RECEIVER OUTPUTS

The ADM14196E has failsafe receiver outputs that assume a high output level if the receiver input is zero or open-circuit

LAPLINK COMPATIBILITY

The ADM14196E can easily provide 128 kbps data rate under maximum driver load conditions of C_L = 2500pF and R_L = 3kΩ at minimum power supply voltages.

MOUSE DRIVING

A typical serial mouse can be powered from the drivers. Two driver outputs connected in parallel and set to VOH can be used to supply power to the V+ pin of the mouse. The third driver is set to VOL to sink current from the V- terminal. Typical mouse specifications are 10mA @ +6V and 5mA @ -6V.

Figure 29. Typical DCE Application

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